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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,401	05/10/2005	Tatsuo Kataoka	1217-051388	2875

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EXAMINER	
MALEK, MALIHEH	
ART UNIT	**PAPER NUMBER**
2813	

MAIL DATE	DELIVERY MODE
10/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/534,401	KATAOKA ET AL.	
	Examiner	Art Unit	
	Maliheh Malek	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/20/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the application filed on 5/10/2005.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in **Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966)**, that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: ***(See MPEP Ch. 2141)***

a. Determining the scope and contents of the prior art;
b. Ascertaining the differences between the prior art and the claims in issue;
c. Resolving the level of ordinary skill in the pertinent art; and
d. Evaluating evidence of secondary considerations for indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1 to 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuura (Pat. No.: US 6,849,950 B1) in view of Fukutomi et al. (Pat. No.: 5,976,912), herein Fukutomi.

Regarding claim 1, Matsuura teaches a film carrier tape for mounting electronic components, which tape comprises an insulating film 106 (col. 1, lines 48-51) and, on the surface thereof, an inner connection terminal 107 (col. 1, lines 30-33), an outer connection terminal 10 (col. 6, lines 13-16) and a wiring for connecting these terminals and further comprises a solder resist layer 103 covered in such a way that the connection terminals are exposed (col. 1, lines 35-38), wherein wiring positioned from a part where the inner connection terminal is electrically connected with the connection terminal of the electronic component to the edge of the solder resist layer and wiring in a 1000 μm length from the edge of the solder resist, which wiring is protected by the solder resist layer, are formed in an almost straight shape (Fig. 1 and col. 1, lines 51-55).

However, regarding claim 1, Matsuura does not teach that the tape secures electric connection of a connection terminal of an electronic component and the inner connection terminal by applying an ultrasonic wave on the inner connection terminal in mounting the electronic component.

In the same field of endeavor, regarding claim 1, Fukutomi teaches a film carrier tape wherein the tape secures electric connection of a connection terminal of an electronic component and the inner connection terminal by applying an ultrasonic wave on the inner connection terminal in mounting the electronic component ([0150], lines 18-20) without having to use additional material.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Matsuura film carrier tape by incorporating the ultrasonic wave bonding method without having to use additional material.

Regarding claim 2, Matsuura teaches a film carrier tape for mounting electronic components wherein the inner connection terminal 7 is a bonding pad, and the connection terminal of the electronic component 2 and the bonding pad are electrically connected by wire bonding 8 using a conductive metal thin wire (Fig. 4 and col. 5, lines 37-54) to provide a highly reliable device with reliable insulation (col. 2, lines 34-38).

Regarding claim 3, Matsuura teaches a film carrier tape for mounting electronic components wherein wiring positioned from the part where the inner connection terminal 107 is electrically connected with the connection terminal of the electronic component 102 to the edge of the solder resist layer 103 and wiring in a 1000 μm length from the edge of the solder resist 103, which wiring is protected by the solder resist layer 103, are formed as to not have an inflection part at which wiring is sharply bended or curved (Fig. 1, col. 5, lines 37-54 and col. 1, lines 51-55) to provide a highly reliable device with reliable insulation (col. 2, lines 34-38).

Regarding claim 4, Fukutomi teaches a film carrier tape for mounting electronic components wherein a wiring pattern comprising the inner connection terminal 13, the outer connection terminal (on chip 3) and the wiring 100 for connecting those connection terminals is formed by selectively etching an

electrodeposited copper foil and at least the crystal structure of the inner connection terminal and the crystal structure of the electrodeposited copper foil for forming the wiring have identity before and after the wire bonding ([0130], Fig. 3a-3f) to have excellent chemical and heat resistance.

Regarding claim 5, Fukutomi teaches a film carrier tape for mounting electronic components wherein the wiring pattern is formed by selectively etching the electrodeposited copper foil having an average thickness of from 5 to 35 μm ([0130], lines 1-8) to have excellent chemical and heat resistance.

Regarding claim 6, Matsuura teaches a film carrier tape for mounting electronic components wherein wiring positioned from the part where the inner connection terminal 107 is electrically connected with the connection terminal of the electronic component 102 to the edge of the solder resist layer 103 and wiring in a 1000 μm length from the edge of the solder resist 103, which wiring is protected by the solder resist layer 103, are formed as to not have an inflection part at which wiring is sharply bended or curved (Fig. 1, col. 5, lines 37-54 and col. 1, lines 51-55) to provide a highly reliable device with reliable insulation (col. 2, lines 34-38).

Regarding claim 7, Fukutomi teaches a film carrier tape for mounting electronic components wherein a wiring pattern comprising the inner connection terminal, the outer connection terminal and the wiring for connecting those connection terminals is formed by selectively etching an electrodeposited copper foil and at least the crystal structure of the inner connection terminal and the

crystal structure of the electrodeposited copper foil for forming the wiring have identity before and after the wire bonding ([0130], Fig. 3a-3f) to have excellent chemical and heat resistance.

Regarding claim 8, Matsuura teaches a film carrier tape for mounting electronic components wherein the wiring pattern is formed by selectively etching the electrodeposited copper foil having an average thickness of from 5 to 35 μm ([0130], lines 1-8) to have excellent chemical and heat resistance.

Regarding claims 1, 3 and 6, Matsuura discloses the claimed invention except for the length of the wiring of 1000 μm. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the length of the wiring to 1000 μm, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA. 1980).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Oya (Pub. No.: 2001/0054753 A1) teaches a package-side land of a semiconductor package that is wholly exposed into the opening of a solder resist layer. The board-side land of the mount board is also wholly exposed into the opening of a solder resist layer.

Shimizu (Pub. No.: US 2003/0089968 A1) teaches a semiconductor device which includes an electrically insulating board; conductive interconnections formed on a first face of the board and on a second face opposite to the first face; a semiconductor chip fixed to the board through at least the interconnections on the first face.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maliheh Malek whose telephone number is (571)270-1874. The examiner can normally be reached on Mon-Fri, 8:30-6pm ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Oct. 22, 2007

MM

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